IN THE SPECIFICATION:

Please amend paragraph **[0002]** as follows:

[0002] In order to conserve the amount of surface area, or "real ~~estate",~~ estate," consumed on a carrier substrate, such as a circuit board, by semiconductor devices connected thereto, various types of increased-density packages have been developed. Among these various types of packages is the so-called "multi-chip module" (MCM). Some types of multi-chip modules include assemblies of semiconductor devices that are stacked one on top of another. The amount of space on a carrier substrate that may be saved by stacking semiconductor devices is readily apparent--a stack of semiconductor devices consumes roughly the same amount of real estate on a carrier substrate as a single, horizontally oriented semiconductor device or semiconductor device package.

Please amend paragraph **[0036]** as follows:

[0036] FIG. 9 is a cross-sectional representation of a stacked assembly that includes the semiconductor ~~devices~~ device of FIGs. 1 and 2;

Please amend paragraph **[0046]** as follows:

[0046] Spacers 22 may be substantially identically configured or have different configurations. By way of example only, spacers 22 may have substantially planar upper surfaces and cross-sectional shapes taken along the length thereof including, but not limited to, round shapes (*e.g.*, circular, ovals, ellipsoids, etc.), polygonal shapes (*e.g.*, triangular, square, ~~diamond shaped,~~ diamond-shaped, rectangular, hexagonal, octagonal, etc.) (see FIG. 4), crosses, elongate members which may be straight, bent, or curved, and other shapes. Alternatively, the upper surfaces of spacers 22 may be nonplanar, such as cones, pyramids, the depicted domes, or other suitable shapes. Spacers 22 may comprise solid or at least partially hollow members.

Please amend paragraph **[0052]** as follows:

[0052] FIGs. 7A-7D schematically depict an exemplary stereolithography process for fabricating spacer layer 20 (FIG. 7D) on an active surface 12 of a semiconductor device 10. As

shown in FIG. 7A, active surface 12 of semiconductor device 10 may be submerged beneath a quantity of unconsolidated material 213″ (*e.g.*, a liquid photoimageable polymer), which forms a layer 215″ over active surface 12. In FIG. 7B, selected regions of layer 215″ are at least partially consolidated, as known in the art (*e.g.*, by exposure of a liquid photoimageable polymer to curing radiation, such as a laser beam 235). The at least partially consolidated portions of layer 215″ form sublayers 22a of spacers 22 of spacer layer 20 (FIG. 7D). This process may be repeated, as shown in FIGs. 7C and 7D, one or more times to form a plurality of at least partially superimposed, contiguous, mutually adhered sublayers 22a, 22b,~~ etc. ~~ etc., of spacers 22. As depicted in FIG. 7D, each spacer 22 includes two sublayers 22a, 22b, although stereolithographically fabricated spacers 22 having single layers or other numbers of sublayers are also within the scope of the present invention.

Please amend paragraph **[0057]** as follows:

[0057] In the illustrated example, back side 14 of first semiconductor device 10 is secured to substrate 40 by way of a suitable adhesive material 15, such as a thermoplastic resin, a silicon-filled thermoplastic resin, a thermoset resin, an epoxy, a silicone, a silicone-carbon resin, a polyimide, a polyurethane, or a parylene. Of course, first semiconductor device 10 may be secured to or otherwise associated with a substrate in a different manner, depending upon the particular type of substrate employed. By way of example only, leads may extend partially over and be secured to active surface 12 of first semiconductor device 10. Such leads may extend over corresponding bond pads 16 and be secured thereto directly (*e.g.*, by thermocompression bonds) or by way of conductive joints (*e.g.*, balls, bumps, pillars, columns, or other structures of a metal or metal alloy, such as solder, a conductive epoxy, a conductor-filled epoxy, or a z-axis conductive~~ elastomer).Alternatively, ~~ elastomer). Alternatively, discrete conductive elements, such as bond wires or TAB elements may be positioned or formed between each lead and its corresponding bond pad 16 to electrically connect the same.

Please amend paragraph **[0059]** as follows:

[0059] Alternatively, the heights of spacers 22 may be about the same as or even smaller than the distances discrete conductive elements 18 protrude above active surface 12, so long as the heights of spacers 22 and the combined strengths of discrete conductive elements 18 over which second semiconductor device 110 is positioned prevent discrete conductive elements 18 from being damaged (*e.g.,* by being bent, kinked, or otherwise deformed) or from collapsing onto one another. If the heights of spacers 22 are less than the distance discrete conductive elements 18 protrude above active surface 12, it is preferred that portions of discrete conductive elements 18 and back side 114 that may contact one another be electrically isolated from each other. By way of example, at least portions of discrete conductive elements 18 may include a dielectric coating 19 thereon. Alternatively, or in addition, all or part of back side 114 may include a dielectric coating 116. Suitable dielectric materials for both dielectric coating 19 and dielectric coating 116 include, but are not limited to, nonconductive polymers, glass, silicon oxide, silicon nitride, and silicon oxynitride, as well as nonconductive oxides of the respective discrete conductive element 18 or <u>second</u> semiconductor device 110 material.

Please amend paragraph **[0062]** as follows:

[0062] FIG. 9C depicts an assembly 130 that includes <u>first and second</u> semiconductor devices 10, 110, as well as spacers 22 and adhesive material 115 therebetween, that are similar to those of assembly 30 depicted in FIG. 9. Assembly 130 differs from assembly 30 in that substrate 140 comprises leads 142. As depicted, leads 142 are of a leads-over-chip (LOC) configuration and, thus, extend partially over and are secured to an active surface 12 of first semiconductor device 10. In addition, leads 142 are positioned at least partially over and bonded to corresponding bond pads 16 of first semiconductor device 10. By way of example only, leads 142 may be bonded to corresponding bond pads 16 by way of thermocompression bonds or by the use of a conductive adhesive material, such as solder, another metal or metal alloy, conductive or conductor-filled epoxy, an anisotropically conductive elastomer, or the like, between leads 142 and bond pads 16. Alternatively, LOC type leads 142 may communicate with corresponding bond pads 16 by way of discrete conductive elements (*e.g.,* bond wires, TAB

elements, etc.). Other variations of the assemblies depicted herein may include substrates that comprise other types of leads, circuit boards, an additional semiconductor device, or the like.

Please amend paragraph **[0065]** as follows:

[0065] Referring again to FIG. 9, an exemplary process for forming assembly 30 includes securing a first semiconductor device 10 to a substrate 40. As depicted, an adhesive material 15 is used, although other known methods for securing semiconductor devices to substrates are also within the scope of the present invention. Known processes may be used to form or position discrete conductive elements 18, such as TAB elements, thermocompression bonded leads, the depicted bond wires, or the like, between bond pads 16 of first semiconductor device 10 and corresponding contact areas 46 of substrate 40. Spacers 22 may be formed on regions of active surface 12 of semiconductor device 10 by known processes, such as those described previously herein with reference to FIGs. 5-8. The formation of spacers 22 may be effected before or after first semiconductor device 10 is secured to substrate 40, as well as before or after the formation of discrete conductive elements 18. A second semiconductor device 110 is positioned over spacers 22, with a back side 114 thereof resting against spacers 22.

Please amend paragraph **[0066]** as follows:

[0066] Optionally, a suitable adhesive material 115, such as a known underfill material, may be introduced into voids 24 of spacer layer 20, between active surface 12 of first semiconductor device 10 and back side 114 of second semiconductor device 110. When spacers 22 at least partially encapsulate discrete conductive elements 18, as depicted in FIG. 10, spacers 22 may prevent discrete conductive elements 18 from being collapsed onto one another, bent, kinked, or otherwise distorted or damaged during the introduction of adhesive material 115 between first and second semiconductor devices 10 and 110. One or more known processes may be used to at least partially cure or otherwise harden adhesive material 115. Spacers 22 that at least partially encapsulate discrete conductive elements 18 may also electrically isolate discrete conductive ~~elements~~ elements 18 from the back side 114 of an adjacent semiconductor device 110.

Please amend paragraph **[0068]** as follows:

[0068] Turning now to FIG. 12, a package 50 incorporating teachings of the present invention may include any assembly (*e.g.*, assemblies 30, 30′, 30″) according to the present invention. As illustrated, package 50 includes assembly 30, as well as an encapsulant 52 substantially filling voids 24 in spacer layer 20 and surrounding <u>first and second</u> semiconductor devices 10 and 110, discrete conductive elements 18, and portions of substrate 40 that are located adjacent to <u>first</u> semiconductor device 10. Alternatively, encapsulant 52 may be formed separately from a layer of adhesive material 115 (*see, e.g.*, FIG. 9) between first semiconductor device 10 and second semiconductor device 110.

Please amend paragraph **[0069]** as follows:

[00069] While encapsulant 52 is depicted as being formed by transfer molding processes or by pot molding processes and, thus, from appropriate compounds (*e.g.*, a silicon-filled thermoplastic resin for transfer molding or an epoxy for pot molding), other encapsulation techniques, such as glob top processes, and appropriate materials may also be used to form encapsulant 52. Although encapsulant 52 may be formed separately from the layer of adhesive material 115 between first and second semiconductor devices 10 and 110, the same or similar materials may be used as adhesive material 115 and to form encapsulant 52. Likewise, adhesive material 115 and/or the material of encapsulant 52 may comprise the same or a similar material to that from which spacers 22 are formed. Use of the same or similar materials for these elements may ~~optimized~~ <u>optimize</u> adhesion and provide for a matched coefficient of thermal expansion (CTE).

Please amend paragraph **[0070]** as follows:

[0070] Package 50 may also include external connective elements 54 electrically coupled to <u>corresponding</u> contact areas 46 by vias and/or conductive traces (not shown) carried by substrate 40, as known in the art. External connective elements 54 may, by way of example only, comprise conductive plug-in type connectors, pin connectors, conductive or

conductor-filled epoxy pillars, an anisotropically conductive adhesive, the depicted conductive bumps, or any other conductive structures that are suitable for interconnecting assembly 30 with other, external electronic components.